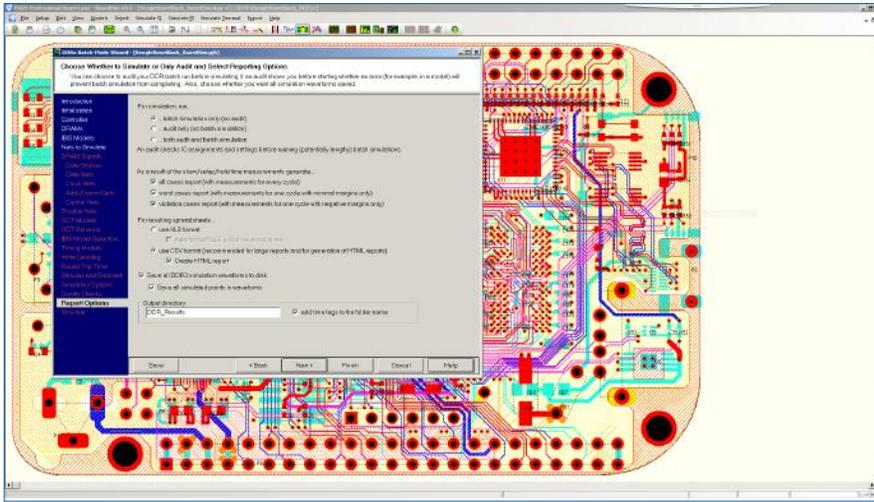


HyperLynx DDR PE

D A T A S H E E T



The simple wizard-based interface makes it easy to set up DDR1/2/3 simulations.

Overview

HyperLynx® DDR PE was created especially for Altium, Allegro, CADSTAR, and OrCAD engineers who need powerful analysis of DDR1, DDR2, DDR3, and LPDDR 1/2/3 designs.

HyperLynx DDR PE provides powerful analysis for PCBs with DDR memory, greatly reducing validation and debug cycles. Easily report setup/hold times, overshoot/undershoot, and non-monotonicity in your DDR interface to improve design quality. Measurements can be validated against JEDEC DDR1/2/3 standard values or custom operating points. The detailed simulations take into account board-level effects, such as lossy transmission lines, reflections, impedance changes, effects of vias, ISI, crosstalk, and timing delays, providing a comprehensive view of your memory interface.

MAJOR BENEFITS:

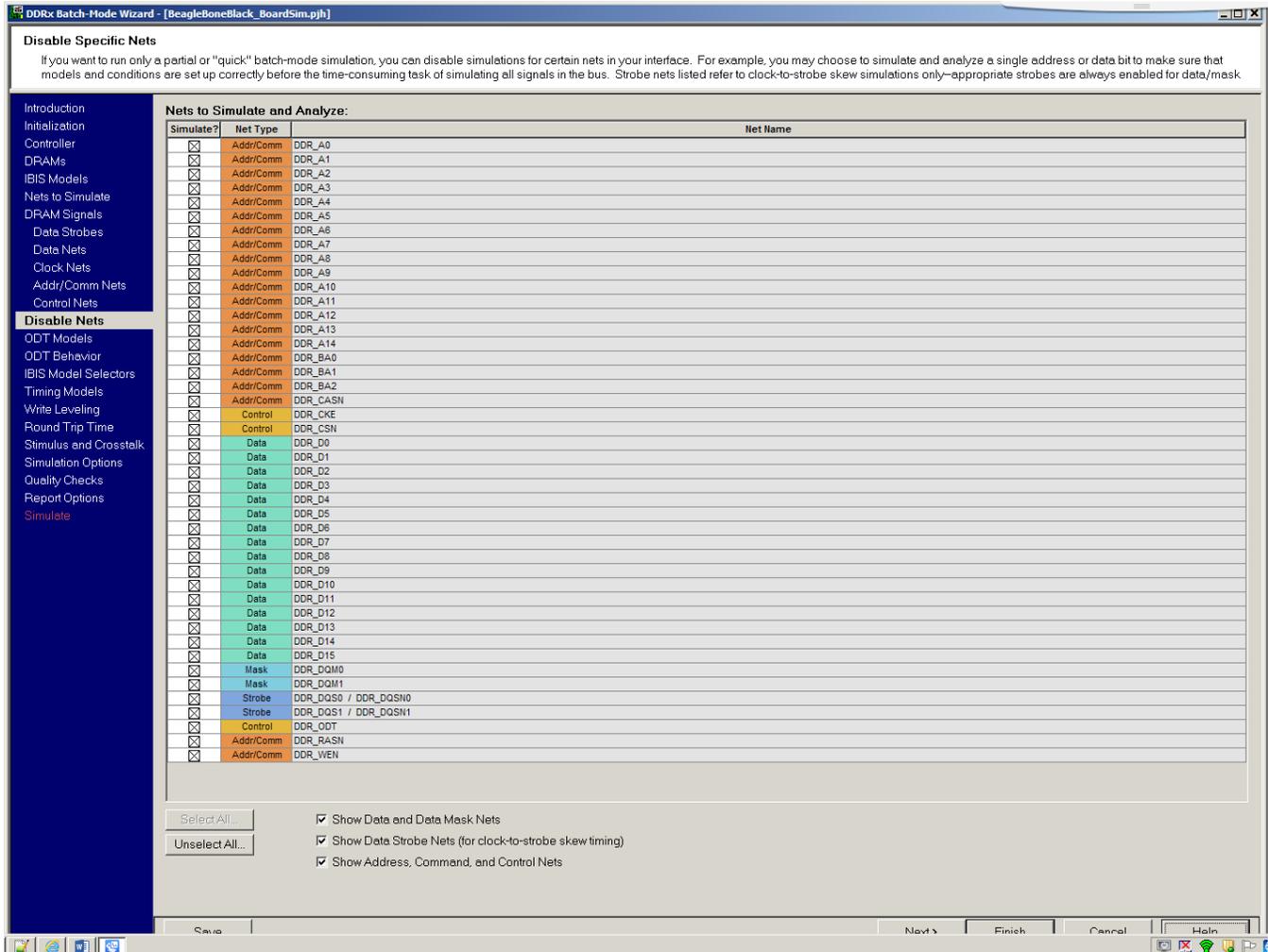
- Wizard-based interface helps analyze DDR1, DDR2, and DDR3 designs, including low-power variants
- Simulate with any number of DRAM devices, from single-memory to multiple-memory modules/slots
- Characterize Signal Integrity (SI) and system-level timing with setup/hold and derating calculations per JEDEC or custom standards
- Includes an HTML-based report with details of timing and SI results
- Supports Altium Designer, OrCAD, Allegro, and CADSTAR

Easy Setup with DDRx Wizard

The HyperLynx DDRx Wizard prompts you with all the key questions necessary to set up simulations, from the simplest DDR designs to the most complicated. Users answer relevant information from a choice of IBIS models for controller and memory devices to drive-strength

values for read/write cycles, On-Die-Termination (ODT) settings, and byte-lane / strobe / mask assignment.

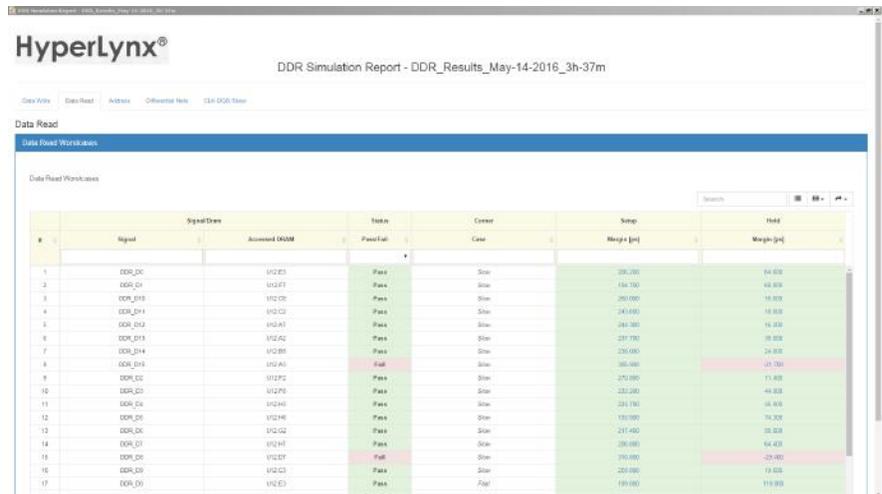
Wizard configurations can be saved and recalled for future use, allowing you to create templates that simulate exactly what you want for use on future designs.



Extensive options in the DDRx Wizard give you flexibility in configuring a DDR simulation.

HTML-Based Reports

The DDRx Wizard generates a clean, intuitive report at the end of the simulation process, including pass/fail data, per the information in your wizard-based configuration. Results can be filtered, letting you explore both timing and SI concerns across data read/write cycles, on the address/command bus, or by differential nets. PADS HyperLynx DDR greatly reduces the setup time required for successful simulations while providing detailed results that can help drive decisions in your design process.



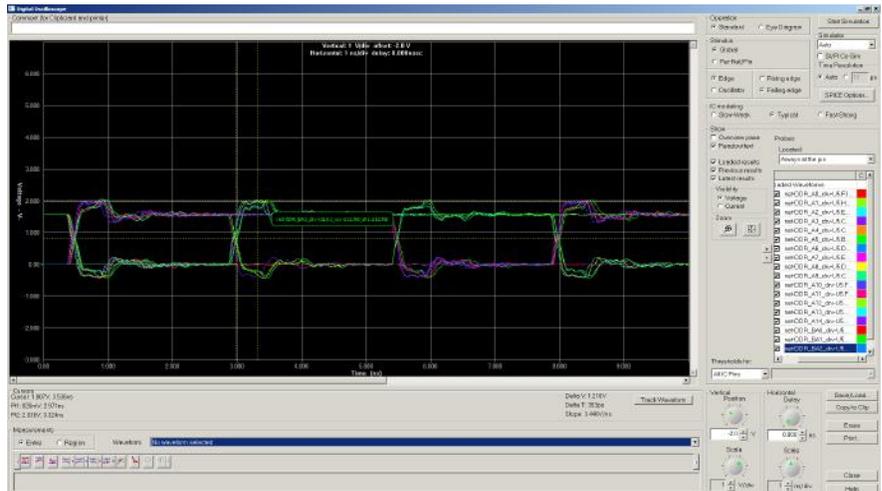
HyperLynx[®] DDR Simulation Report - DDR_Results_May-14-2016_3h-37m

#	Signal	Accessed DQ/DQ#	Pass/Fail	Case	Setup	Margin [ps]
1	DDR_D0	UQ2E3	Pass	Slow	200,000	64.000
2	DDR_D1	UQ2F7	Pass	Slow	150,700	63.000
3	DDR_D10	UQ2D9	Pass	Slow	260,000	16.000
4	DDR_D11	UQ2D8	Pass	Slow	243,000	16.000
5	DDR_D12	UQ2A7	Pass	Slow	240,000	16.000
6	DDR_D13	UQ2A2	Pass	Slow	227,700	39.000
7	DDR_D14	UQ2B9	Pass	Slow	230,000	24.000
8	DDR_D15	UQ2A0	Fail	Slow	365,000	45.700
9	DDR_D2	UQ2F2	Pass	Slow	270,000	11.000
10	DDR_D3	UQ2F6	Pass	Slow	320,000	44.000
11	DDR_D4	UQ2A6	Pass	Slow	221,100	16.000
12	DDR_D5	UQ2A6	Pass	Slow	180,000	76.300
13	DDR_D6	UQ2D2	Pass	Slow	217,400	35.000
14	DDR_D7	UQ2H7	Pass	Slow	330,000	64.000
15	DDR_D8	UQ2D7	Fail	Slow	190,000	25.000
16	DDR_D9	UQ2D3	Pass	Slow	230,000	12.000
17	DDR_D0	UQ2E3	Pass	Fast	190,000	119.000
18	DDR_D1	UQ2F7	Pass	Fast	140,000	119.000

An HTML report makes it easy to intuitively examine results and spot failures. Data can be exported in a variety of formats, according to your needs.

Detailed, Interactive SI Analysis

Batch-mode simulation data created by the DDRx wizard can be saved to disk, so users can examine several nets simultaneously for detailed SI problems offline, using the HyperLynx oscilloscope. Users can interactively place cursors and take notes of overshoot, undershoot or signal timing.



Load any number of signals from batch-mode results into an interactive oscilloscope to take detailed measurements.

Summary

DDRx bus validation involves the analysis of several timing and voltage measurements. Manual analysis of an entire DDR bus is impractical and error prone. HyperLynx DDR PE greatly reduces the setup time required for successful simulations while providing detailed results that can help drive decisions in your design process.

For the latest product information, call us or visit: www.mentor.com

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