HyperLynx
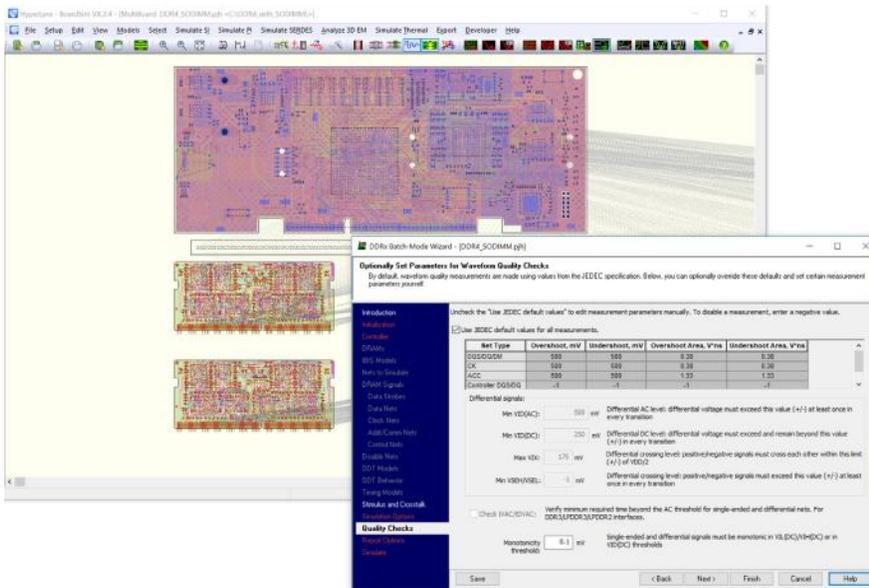## DDRx Design & Verification

Overview

HyperLynx® DDRx provides powerful integrated signal integrity, crosstalk, and timing analysis that significantly reduces design and debug cycles for PCBs with DDRx memory. Extensive pre-layout, what-if simulations are used to define PCB layout and routing constraints that are driven into the PCB layout flow. Automated post-route simulations extract 'as-routed' circuit topologies from PCB databases to perform comprehensive full-interface analysis, validating all signals, groups, and timing relationships at a detailed level before the PCB is sent to manufacturing.

When used with Mentor's Xpedition® flow, HyperLynx DDRx makes it easy to pass pre-layout constraints to PCB layout. Routed designs can then be driven from the Xpedition layout editor directly back into HyperLynx for analysis. The unique HyperLynx DDRx wizard guides users through all stages of the setup and simulation process, making complex DDRx analysis accessible to users who aren't full-time SI experts.

KEY FEATURES:

- Automated pre-/post-route work flow for determining DDRx interface voltage and timing margins

- Integrated signal integrity, crosstalk, and system-level timing analysis of all signal groups and their relationships

- Integrated support for JEDEC measurement and derating data

- Calculates DQS/CLK write-leveling delays and per-bit/per-byte calibration delays for DQ/DQS signals

- Supports power-aware modeling of signal/power delivery network (PDN) interactions including SSN, via-to-via coupling and non-ideal return path effects

- Eye diagram viewer displays signals and their associated signal integrity/timing metrics

- Creates eye diagrams masks placed relative to DQS/CLK edges for DDR4/LPDDR4 interfaces

- Provides native design import from Xpedition and industry-standard import formats for Altium® Designer, OrCAD®, Allegro®, and CADSTAR®

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Powerful modeling and simulation

Fully validating a DDRx interface requires signal integrity and crosstalk simulation to be run on all signals, signal-quality requirements and thresholds to be verified for each signal, and all timing relationships between individual signals and their respective groups to be analyzed. Performed comprehensively, this requires hundreds of SI simulations, thousands of individual signal quality and timing measurements, the incorporation of signal derating based on JEDEC standards, and the calculation and roll-up of individual, byte-lane and signal-group-level voltage and timing margins.

JEDEC defines signal quality and timing specifications for DRAM devices, although device vendors can exceed those values for high-performance components. Generally, DRAM simulation models are device-specific, while JEDEC timing parameters are used for everything except special high-performance parts. Controller simulation models and timing parameters, by contrast, are always component-specific, as JEDEC standards do not apply to DRAM controllers.

```
/************************************************************
 *  Derived timing parameters
 ************************************************************/
    parameter tDQBit = `tCK / 2;          // Data bit time
    parameter tDQPrelaunch = -tDQBit/2;   // Data bit pre-launch shift (Write to DRAM)
    parameter tACDlyMin = `tCK/2 - tACCSkew;  // Delay from CK rising out to Addr/Cmd/Ctl invalid (min)
    parameter tACDlyMax = `tCK/2 + tACCSkew;  // Delay from CK rising out to Addr/Cmd/Ctl invalid (max)

    parameter tCTLMin = -`tCK + tACDlyMin;    // CK rising out to earliest valid CTL (CK-1)
    parameter tCTLMax = -`tCK + tACDlyMax;    // CK rising out to latest valid CTL (CK-1)

`ifdef ADDRCMD1T
    parameter tACMin = -`tCK + tACDlyMin;     // CK rising out to earliest valid ADDR/CMD (CK-1)
    parameter tACMax = -`tCK + tACDlyMax;     // CK rising out to latest valid ADDR/CMD (CK-1)
`else `define ADDRCMD2T
    parameter tACMin = -(2*`tCK) + tACDlyMin; // CK rising out to earliest valid ADDR/CMD (CK-2)
    parameter tACMax = -(2*`tCK) + tACDlyMax; // CK rising out to latest valid ADDR/CMD (CK-2)
`endif
```

HyperLynx DRAM timing model

DRAM and controller buffer models are typically provided in standard IBIS format. Since there is no standard format for specifying device timing, HyperLynx uses timing models based on the Verilog language. HyperLynx DDRx includes DRAM timing models for different JEDEC standards and speed grades. Sample timing models are provided for controllers and a graphical timing model editor makes it easy to create timing model for specific controllers.

DDRx designs typically start simple and get refined as the design progresses. The first simulations are used to sketch interconnect length, basic device programming and intended routing topologies. As the design progresses, additional signals are added to study the effects of crosstalk and to drive decisions as to how closely signals should be spaced and how much parallelism can be tolerated for a particular distance. For this reason, HyperLynx DDRx allows users to trade off modeling accuracy versus analysis speed, using basic modeling

techniques at the beginning of the design cycle and increasing accuracy and detail as the design progresses.

For example, initial simulations typically disable signal coupling due to crosstalk, because if an interface doesn't work without crosstalk, it certainly won't work with crosstalk. Since the inclusion of crosstalk effects increases both model generation and simulation times, there's no point including crosstalk until the design passes without it. The same is true for other physical phenomena. HyperLynx uses a variety of 2D and 3D solvers for interconnect modeling, letting users tailor the level of accuracy to their individual needs. Individual phenomena can be included or excluded from simulation, letting users isolate and quantify individual impacts on system voltage and timing margins. These techniques help maximize designer productivity by improving overall throughput.
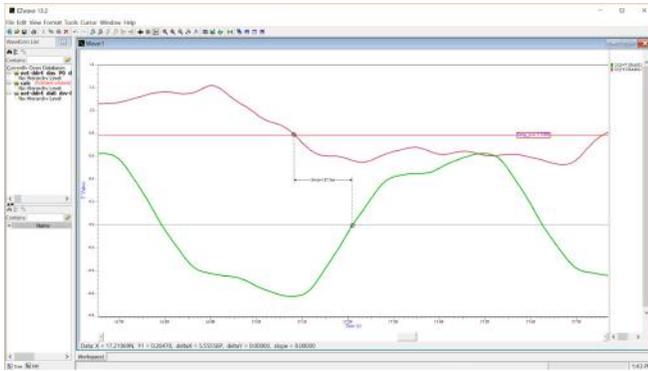
Comprehensive results reporting

HyperLynx DDRx analysis creates a HTML report that lists the pass/fail status of individual signals along with voltage and timing margins. This multi-tabbed report is divided into sections for data read, data write, address net, differential net, CLK-DQS skew relationships and simulation setup information. Users can launch an eye diagram viewer from within the report that displays eye plots and bit error rate (BER) plots along with their associated simulation metrics. All signals and their metrics are shown in a spreadsheet format, which can be filtered to zero-in on selected sets of results. Simply click a measurement to open the waveform and zoom in on an area of interest.
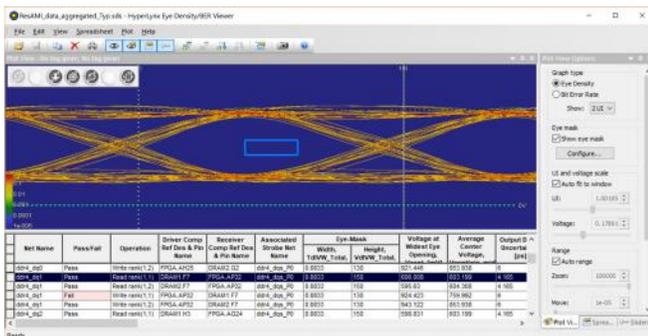

*A searchable HTML report makes it easy to examine results and spot failures.*

Signal metrics in the report can be hyperlinked to display a graphical view of the measurement.

Access the eye-diagram viewer, with complete signal-quality and timing metrics, directly from the HTML results spreadsheet.

Automated workflow

Comprehensive DDR interface analysis is a complex, multi-step process that requires detailed definition of the DDR standard being analyzed, the interface and DRAM DIMM architecture, the target data rate, the dynamic termination settings, and other parameters. The HyperLynx DDRx wizard guides users step by step through the pre- and post-route analysis workflows, prompting users for the information needed to set up and run simulations, whether they be simple memory-down onboard memory setups or multi-DIMM, multi-rank configurations. Users are guided through the process of selecting IBIS models for controller and memory devices, specifying drive-strength and On-Die-Termination (ODT) settings for read/write cycles, and defining byte-lane / strobe/mask assignments. Wizard settings can be saved and reused as templates for simulating future designs.
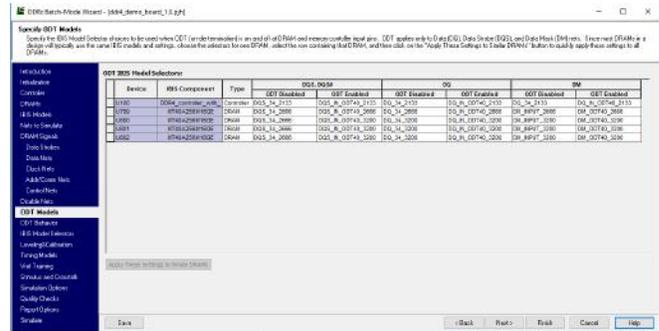
The HyperLynx DDRx wizard guides users step by step through the setup of complex simulation projects.

Because there are no standard formats for specifying timing data for DDR controllers, HyperLynx also provides a Timing Model Wizard for capturing controller timing data and creating a timing model.
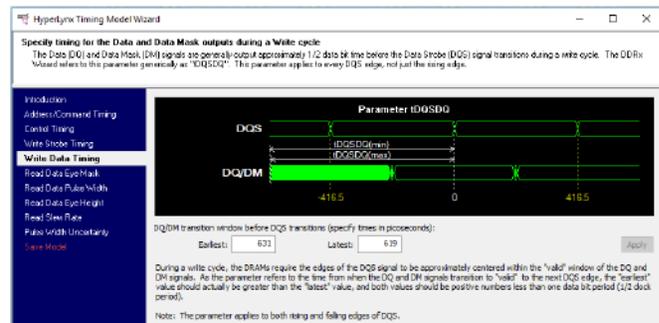
The HyperLynx timing model wizard makes it easy to create controller models and modify DRAM models.

Pre-route analysis drives design constraints

The HyperLynx DDRx wizard is used during pre-route analysis to develop detailed routing rules that will drive physical design. One signal from each net class is used to represent its corresponding bus, with additional nets added to determine the impact of crosstalk on voltage and timing margins. Individual design parameters can be swept during pre-route analysis to define optimal values for PCB layout rules and device configuration at system power-up.

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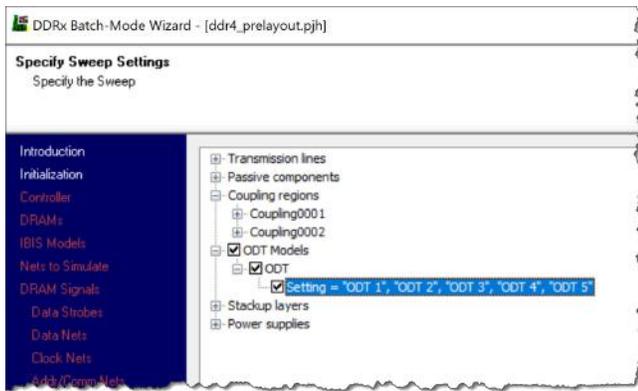
The DDRx wizard can sweep parameters to determine optimal design rules and settings.

Once the optimal design rules are identified, users can create templates to drive routing topologies and rules directly back into Xpedition. The data can also be exported in formats ready for import into other PCB layout systems.
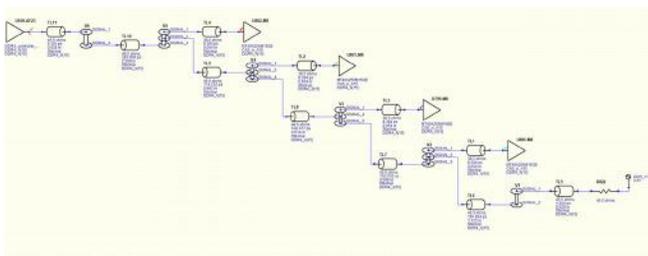

DDR4 address routing template.
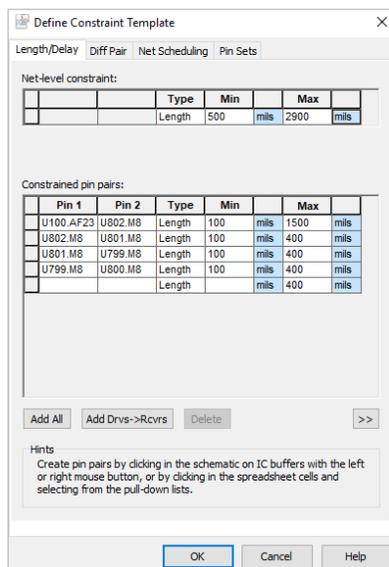
Routing constraints for DDR4 address routing.

Post-route analysis / full interface-level verification

After the PCB is routed, the wizard extracts detailed as-routed topologies for each net and simulates all signals and groups. Crosstalk coupling can be included or excluded, depending on the desired level of detail, and coupled nets can be selected either by physical distance or electrical coupling criteria. When nets are selected interactively for simulation, nets that meet the coupling thresholds are automatically selected for simulation and shown in the PCB view. This is a very powerful way to scan PCB databases for unexpected coupling.
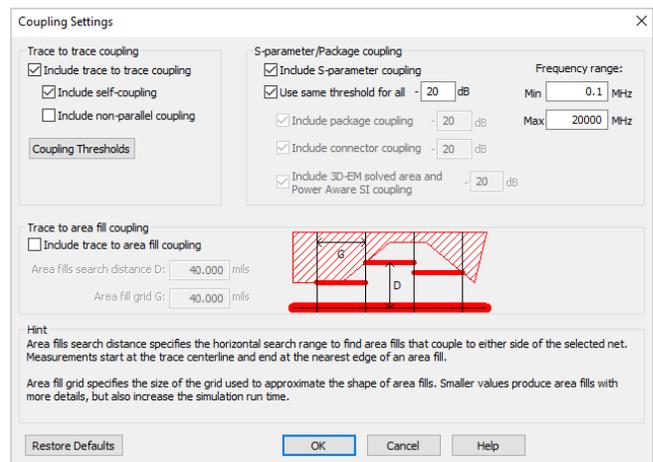
*Coupling thresholds can be specified using physical or electrical criteria.*
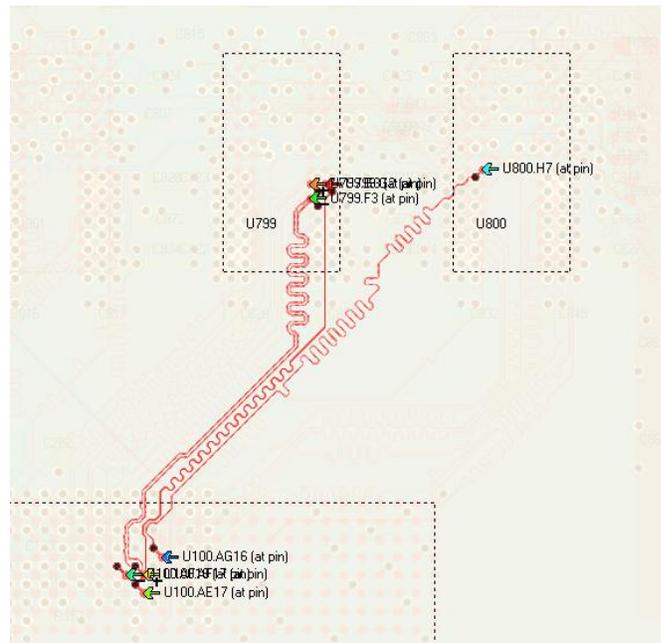
When a net is selected interactively, coupled nets are also displayed.

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Post-route analyses can involve hundreds of simulations and take full advantage of multi-core/multi-threaded CPUs to accelerate simulation throughput. Simulation results for every signal are automatically post-processed to analyze all signal integrity and timing relationship requirements across the full interface. This comprehensive level of simulation can be used to sign off a board before release to manufacture.

Power-aware analysis

Interactions between a system's Power-Delivery Network (PDN) and high-speed signals degrade signal quality, impacting system voltage and timing margins. The interactions can occur as Simultaneous Switching Noise (SSN), via-to-via coupling through power plane cavities, or as discontinuities in a signal's current return path. Most signal integrity tools ignore these effects and assume ideal PDN behavior instead (see 'A' below). HyperLynx can include these effects in post-route simulation by using integrated 3D EM solvers to create highly detailed models of high-speed traces and their interactions with power planes, and by using IBIS power-aware models to accurately represent the driving device's demand for supply current to support switching events. See 'B' below.
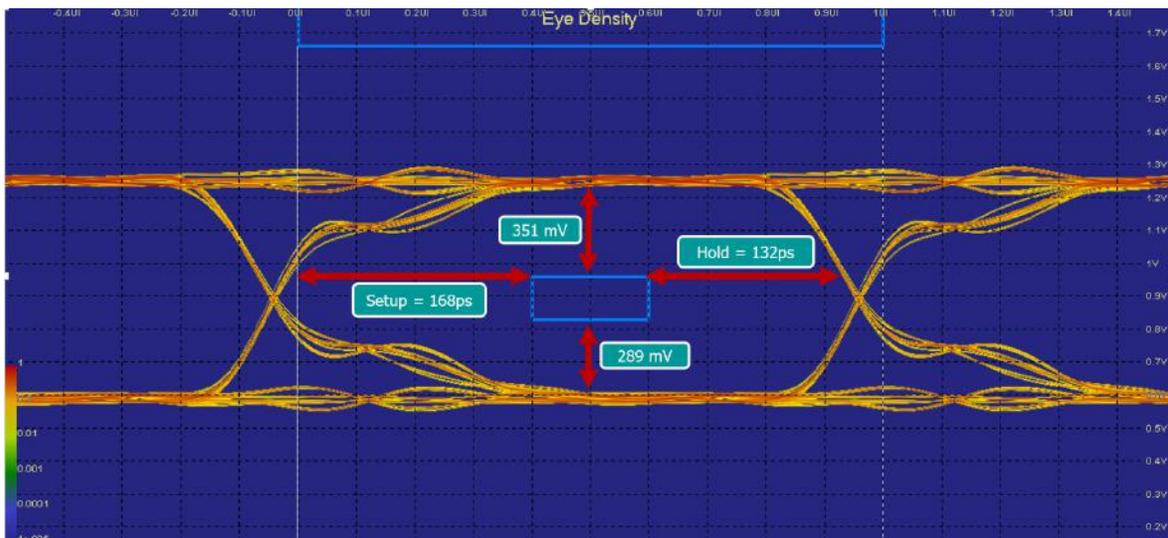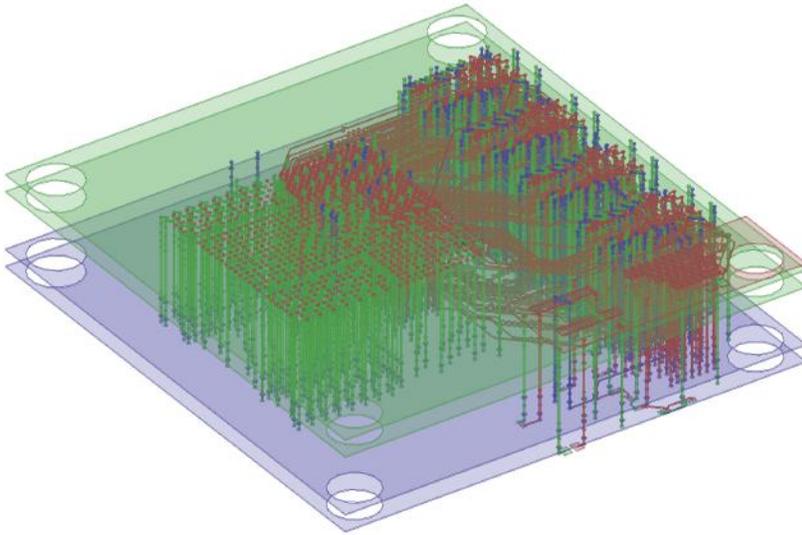

A: Signal behavior without power-aware analysis (an idealized PDN).
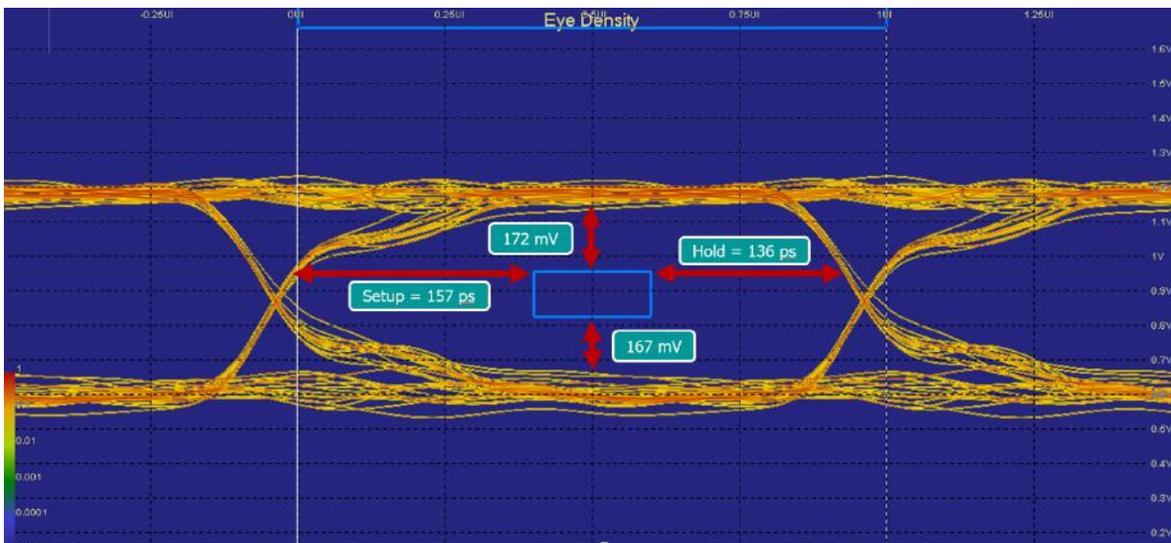
B: Signal behavior with power-aware analysis (an actual PDN).

HyperLynx can include these effects in post-route simulation by using integrated 3D EM solvers to create highly detailed models of high-speed traces and their interactions with power planes, and by using IBIS power-aware models to accurately represent the driving device's demand for supply current to support switching events.

Previously, this type of highly sophisticated analysis was inaccessible to all but a small number of highly skilled SI specialists. Today, HyperLynx makes this capability available to a much broader set of users by integrating dedicated 3D EM solvers into the HyperLynx flow and using the DDRx wizard to automate the analysis process.

Summary

DDR interfaces are some of the most complicated parallel interfaces in use today. Complete validation of DDRx interfaces requires hundreds of signal integrity simulations and thousands of detailed measurements, followed by a comprehensive analysis of all signal quality requirements and signal/group timing relationships. Traditional signal integrity batch-mode tools just aren't up to the task.

HyperLynx streamlines DDRx design by dramatically reducing simulation setup time while providing accurate detailed results that include the effects of lossy transmission lines, reflections, impedance changes, vias, ISI, crosstalk, via-to-via coupling, SSN, and timing delays. With HyperLynx DDRx, you can fast-track design decisions, improve engineering efficiency, and accelerate time to market.

3D EM model used for power-aware analysis.

For the latest product information, call us or visit: w w w . m e n t o r . c o m / h y p e r l y n x