

Schematic Integrity AI analysis

March 2023

Errors in schematic design

- ⚠ Among main sources of reliability issues in the newly released products.
- ⚠ Cause additional time expenses on testing, debugging, redesign, prototyping, bring ups.
- ⚠ Delay products release and postpone start of next projects.
- ⚠ Make post-production maintenance of products hard as hell.



On average boards undergo **2.9** respins due to **insufficient analysis**



The average time to complete a respin is 16 days



The average total cost of a respin is **€26.5K**



If you get your board **right the first time** you save **36 days and €76.9K**

Traditional schematic review process

MANUAL CROSS-CHECKING

- Required effort depends strongly on design complexity.
- Requires investing an enormous amount of engineer's time without actual value generation.
- Consists of hard and monotonous tasks that are not always appreciated by engineers.
- The result is still dependent on a human's mood, involvement, and motivation.
- In general, leaves enough space for multiple mistakes to be missed.

AVAILABLE AUTOMATED SOLUTIONS

- Require significant labor effort for verification prep actions, i.e., building a database of components.
- Require multiple days or weeks of calendar time before the report is released.
- Not self-evolving quality-wise without redefining algorithms manually by humans and manual refilling the database of components.
- Cost 5-20 times higher than schematic integrity AI analysis by Sintecs.

Schematic integrity AI analysis

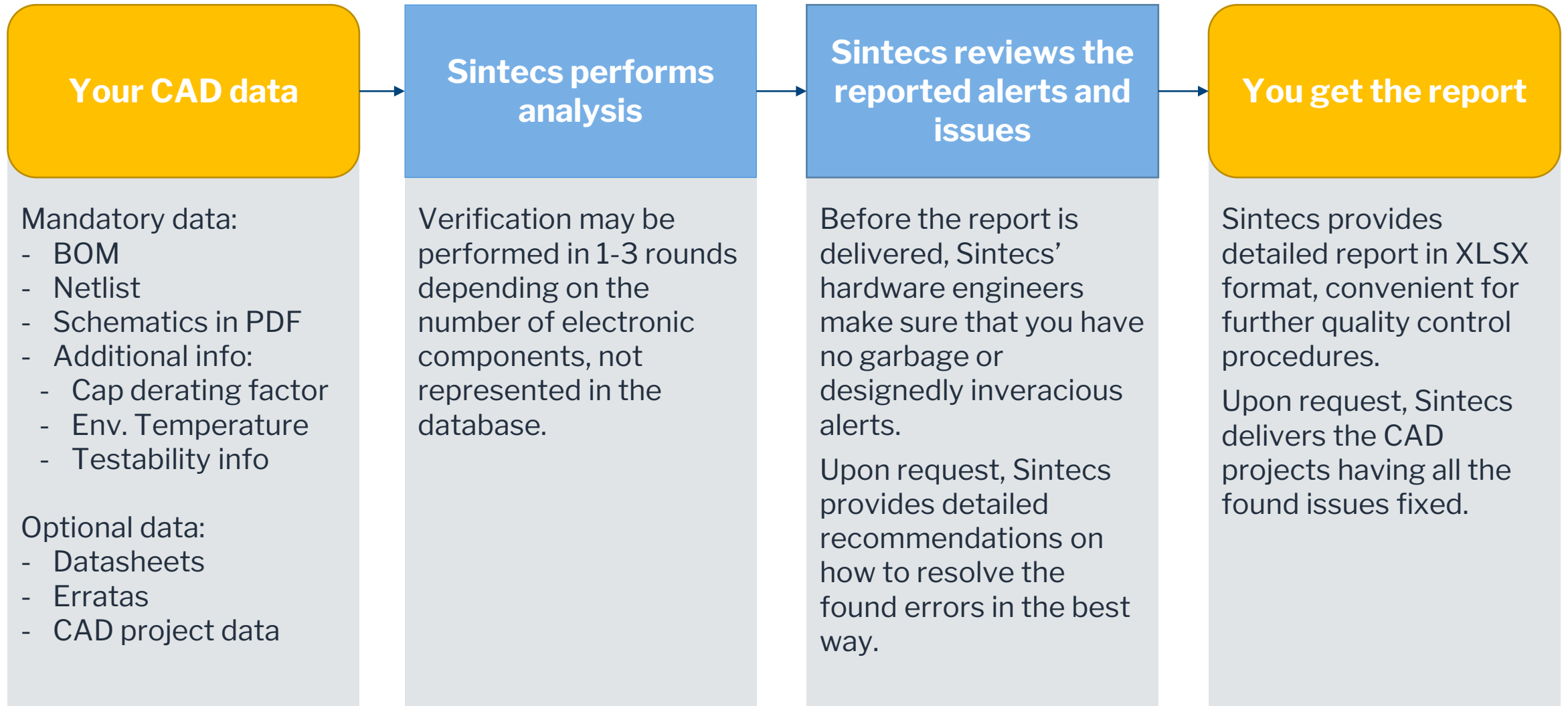
sintecs.eu

Sintecs provides partners and companies worldwide with AI-based schematic integrity analysis, which offers an ideal solution for minimizing errors in schematic designs. Our service combines the benefits of both automated and manual schematic verification while avoiding their downsides:



- No need for lengthy and labor-intensive database preparation.
- Swift report delivery.
- Reports are pre-processed by highly skilled Sintecs engineers.
- Affordable pricing without dependence on design complexity.
- Access to additional quality and design-related services from Sintecs.

Basic workflow



Types of errors under analysis

- ✓ Supply voltage higher or lower than the expected levels
- ✓ Violations of direct connection instructions, including identification of a missing decoupling capacitor on a pin
- ✓ Wrong connections of differential lines
- ✓ Expected and missing pull-up or pull-down resistor
- ✓ Floating pins, including “Enable” or “Reset”
- ✓ Incompatible logical levels between ICs
- ✓ Expected capacitor breach due to over-voltage
- ✓ Activity levels mix-up, including active-high pins shortened to GND
- ✓ Testability check (in case of full or partial ICT testing coverage)
- ✓ Components’ temperature statistics, incl. inadequate component’s ambient operating temperature range
- ✓ General verification of passive component if connected correctly, with no floating pins
- ✓ Transistor misuse, including insufficient voltage on GATE pin
- ✓ I2C/SPI/UART lines mix-up
- ✓ Reset line without capacitor to GND
- ✓ Power-to-GND excessive leakage

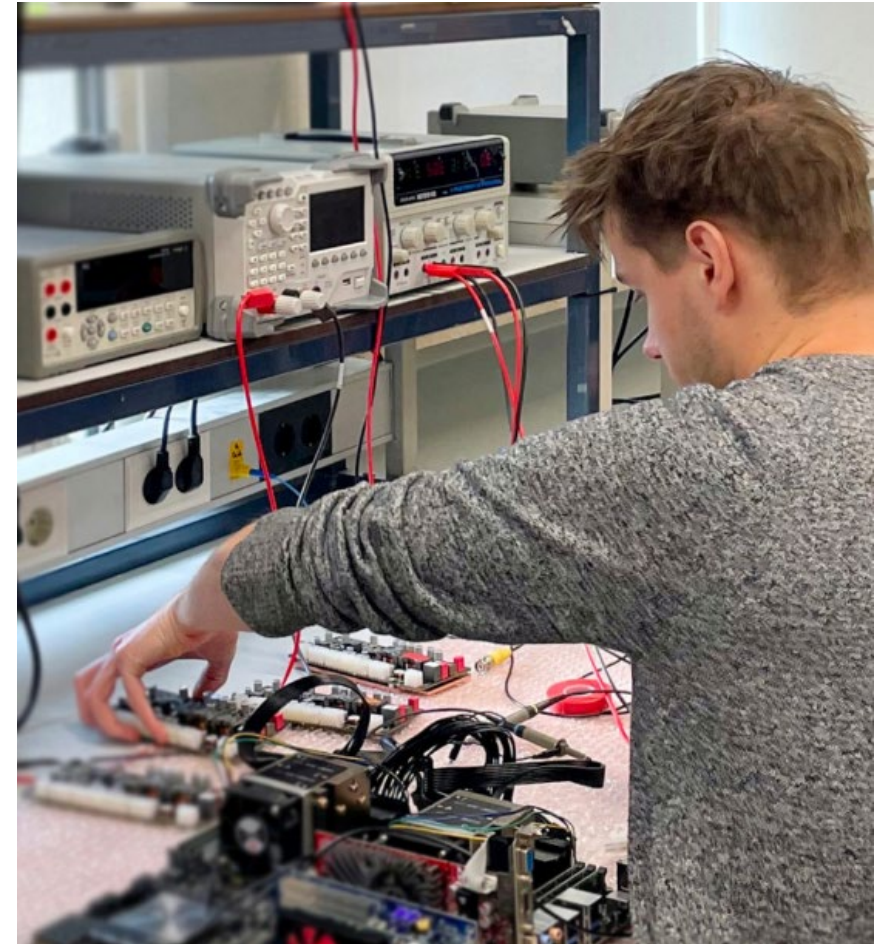
About Sintecs

sintecs.eu

Sintecs is an established leader in the high-speed electronics industry, with over 23 years of experience in signal and power integrity, PCB layout, embedded software, and hardware engineering. We specialize in providing exceptional support for electronic designs, from ideation to the creation of a First-Time-Right prototype for your new product.

Our engineers possess an immense level of expertise, honed over many years of successful project delivery, which we bring to bear on every project we undertake. We are dedicated to ensuring our clients' complete satisfaction. Contact us today to see how we can help you achieve your electronic design goals.

Video: [Sintecs, Designing on the edge](#)



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